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APPLICATION FOR LETTERS PATENT

Title : SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

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CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2003-053330, filed on February 28, 2003, the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

[Field of the Invention]

The present invention relates to a semiconductor device successfully reduced in the off-leakage current, and a method of fabricating the semiconductor device.

[Description of the Related Art]

Recent demands for downsizing of chips have accelerated shortening of gate length of MOS transistors. Short-gate-length MOS transistors are used for battery-powered electronic appliances such as cellular phones, for which a small off-leakage current is an essential feature, and have extension layers and pocket layers formed therein by using As, having a small coefficient of diffusion, as an N-type impurity. More specifically, As is used as an N-type impurity in the pocket layers of P-channel (PMOS) transistor, and extension layers of N-channel (NMOS) transistors. For the purpose of suppressing short-channel effect, and in particular of suppressing generation of off-leakage current and lowering in threshold voltage, which are possibly accompanying the shortening of the gate length, one known conventional method is to raise impurity concentration in the channel.

In this method applied to fabrication of an NMOS transistor, first as shown in Fig. 22A, a gate insulating film 102 and a gate electrode 103 are formed on a semiconductor substrate 101 having a P-type well already formed therein. Next, as shown in Fig. 22B, boron (B) ions are implanted to the semiconductor substrate 101 to thereby form in the surficial portion thereof a P-type pocket layer 104. The ions are implanted by oblique ion implantation which is effected from four directions normal to one another in a plan view, at an implantation energy of 5 to 10 keV, and a dose per direction of 3×10^{12} to 1.8×10^{13} cm^{-2}. Next, as shown in Fig. 22C, arsenic (As) ions are implanted to the pocket layer 104 to thereby form in the surficial portion thereof an N-type extension layer 106. The ion implantation at this time is effected from the direction normal to the surface of the semiconductor substrate 101. The implantation energy is set to 2 to 5 keV, and the dose to 5×10^{14} to 3×10^{15} cm^{-2}. Thereafter a deep N-type source-and-drain diffusion layer and so forth are formed, to thereby complete the NMOS transistor.

On the other hand, in this method applied to fabrication of a PMOS transistor, first as shown in Fig. 23A, a gate insulating film 132 and a gate electrode 133 are formed on a semiconductor substrate 131 having an N-type well already formed therein. Next, as shown in Fig. 23B, arsenic (As) ions are implanted in the semiconductor substrate 131 to thereby form in the surficial portion thereof an N-type pocket layer 134. The ions are implanted by oblique ion implantation which is effected from four directions normal to one another in a plan view, at an implantation energy of 40 to 80 keV, and a dose per

direction of 3×10^{12} to 1.5×10^{13} cm^{-2}. Next, as shown in Fig. 23C, B ions are implanted to the pocket layer 134 to thereby form in the surficial portion thereof a P-type extension layer 136. The ion implantation at this time is effected from the direction normal to the surface of the semiconductor substrate 131. The implantation energy is set to 0.2 to 0.5 keV, and the dose to 5×10^{14} to 2×10^{15} cm^{-2}. Thereafter a deep P-type source-and-drain diffusion layer and so forth are formed, to thereby complete the PMOS transistor.

Prior arts are disclosed in Japanese Patent Laid-Open Nos. 11-163157, 5-267331, 6-224381, 6-338591 and 2000-196077.

Raising in the impurity concentration in the channel by forming the pocket layer in recent transistors having a gate length reduced to as short as 100 nm or less, however, intensifies the electric field at the PN junction in the vicinity of the extension layer, and increases band-to-band tunnel leakage between the drain and the body. The tunnel leakage undesirably increases the off-leakage current.

The present invention is conceived considering the above-described problems, and objects thereof reside in providing a semiconductor device capable of fully suppressing the off-leakage current even if the gate length is as short as 100 nm or less, and in providing a method of fabricating the semiconductor device.

SUMMARY OF THE INVENTION

After thorough investigations for solving the above-described subjects, the present inventors reached several embodiments described in the next.

A first semiconductor device according to the present invention comprises: a semiconductor substrate; a gate insulating film and a gate electrode formed on the semiconductor substrate; a pair of first sidewall insulating films formed on the lateral portions of the gate electrode; and a pair of second sidewall insulating films formed so as to sandwich the first sidewall insulating films with the gate electrode, and having a width larger than that of the first sidewall insulating films. In the surficial portion of the semiconductor substrate, a pair of first N-type impurity-diffused layers containing phosphorus are formed at a first depth so as to be self-aligned with respect to the gate electrode and the first sidewall insulating films. In the surficial portion of the semiconductor substrate, a pair of second N-type impurity-diffused layers are formed at a second depth deeper than the first depth so as to be self-aligned with respect to the gate electrode, the first sidewall insulating films and the second sidewall insulating films. Between the pair of second N-type impurity-diffused layers, a pair of P-type impurity-diffused layers are formed so as to respectively be in adjacent to each of the pair of first N-type impurity-diffused layers.

A second semiconductor device according to the present invention comprises: a semiconductor substrate; a gate insulating film and a gate electrode formed on the semiconductor substrate; and a pair of sidewall insulating films formed on the lateral portions of the gate electrode.

In the surficial portion of the semiconductor substrate, a pair of first P-type impurity-diffused layers are formed at a first depth so as to be self-aligned with respect to the gate electrode. In the surficial portion of the semiconductor substrate, a pair of second P-type impurity-diffused layers are formed at a second depth deeper than the first depth so as to be self-aligned with respect to the gate electrode and the sidewall insulating films. Between the pair of second P-type impurity-diffused layers, a pair of N-type impurity-diffused layers containing phosphorus are formed so as to respectively be in adjacent to each of the pair of first P-type impurity-diffused layers.

In a first method of fabricating a semiconductor device of the present invention, first, a gate insulating film and a gate electrode are formed on a semiconductor substrate. Next, a pair of P-type impurity-diffused layers are formed by introducing a P-type impurity into the surficial portion of the semiconductor substrate with using the gate electrode as a mask, and a pair of first sidewall insulating films are formed on the lateral portions of the gate electrode. Here, the pair of first sidewall insulating films may be formed before the pair of P-type impurity-diffused layers are formed. Next, a pair of first N-type impurity-diffused layers are formed at a first depth by introducing at least phosphorus into the surficial portion of the semiconductor substrate with using the gate electrode and the first sidewall insulating films as a mask. Next, a pair of second sidewall insulating films are formed so as to sandwich the first sidewall insulating films with the gate electrode, and so

as to have a width larger than that of the first sidewall insulating films. Next a pair of second N-type impurity-diffused layers are formed at a second depth deeper than the first depth by introducing an N-type impurity into the surficial portion of the semiconductor substrate with using the gate electrode, the first sidewall insulating films and the second sidewall insulating films as a mask.

In a second method of fabricating a semiconductor device according to the present invention, first, a gate insulating film and a gate electrode are formed on a semiconductor substrate. Next, a pair of N-type impurity-diffused layers are formed by introducing at least phosphorus into the surficial portion of the semiconductor substrate with using the gate electrode as a mask. Next, a pair of first P-type impurity-diffused layers are formed at a first depth by introducing a P-type impurity into the surficial portion of the semiconductor substrate with using the gate electrode as a mask. Next, a pair of sidewall insulating films are formed on the lateral portions of the gate electrode. Next, a pair of second P-type impurity-diffused layers are formed at a second depth deeper than the first depth by introducing a P-type impurity into the surficial portion of the semiconductor substrate with using the gate electrode and the sidewall insulating films as a mask.

The present invention can successfully moderate a strong electric field in the vicinity of the channel, and can consequently reduce leakage current between the drain and the semiconductor substrate even if the gate length is 100 nm or shorter, and can thereby reduce the off-leakage current.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view for explaining types of off-leakage current in an NMOS transistor;

Fig. 2 is a graph showing a relation between the channel impurity concentration and off-leakage current in a PMOS transistor;

Fig. 3 is a graph showing relations between channel impurity concentration and off-leakage current, as compared between an As pocket and a P pocket;

Fig. 4 is a graph showing relations of gate length and threshold voltage V_{th} of an NMOS transistor having an As extension layer;

Fig. 5 is a graph showing relations between gate voltage and drain current obtained in the presence of an As extension layer and a 115-nm long gate;

Fig. 6 is a graph showing relations between gate voltage and drain current obtained in the presence of an As extension layer and a 80-nm long gate;

Fig. 7 is a graph showing BD leakage component in the drain current I_d shown in Fig. 6;

Fig. 8 is a graph showing relations between gate voltage V_g and drain current I_d in an NMOS transistor having a P extension layer;

Fig. 9 is a graph showing relations between gate length and threshold voltage V_{th} of an NMOS transistor having a P extension layer;

Fig. 10 is a graph showing relations between gate length and threshold voltage V_{th} of an NMOS transistor having a P extension layer, as compared between presence and absence of a thin sidewall;

Fig. 11 is a graph showing relations between gate length and off-leakage current I_{off} of an NMOS transistor having a P extension layer, as compared between presence and absence of a thin sidewall;

Fig. 12 is a graph showing relations between gate length and threshold voltage V_{th} of an PMOS transistor having an As pocket layer;

Fig. 13 is a graph showing relations between gate voltage and drain current obtained in the presence of an As pocket layer and a 115-nm long gate;

Fig. 14 is a graph showing relations between gate voltage and drain current obtained in the presence of an As pocket layer and a 80-nm long gate;

Fig. 15 is a graph showing BD leakage component in the drain current I_d shown in Fig. 14;

Fig. 16 is a graph showing relations of gate voltage V_g and drain current I_d of a PMOS transistor (gate length: 80 nm) having a P pocket layer;

Fig. 17 is a graph showing relations of gate voltage V_g and drain current I_d of a PMOS transistor (gate length: 115 nm) having a P pocket layer;

Fig. 18 is a graph showing relations of gate length and threshold voltage V_{th} of a PMOS transistor having a P pocket layer;

Fig. 19 is a graph showing relations between As ratio and off-leakage current;

Figs. 20A to 20G are sectional views sequentially showing process steps of a method of fabricating an NMOS transistor according to a first embodiment of the present invention;

Figs. 21A to 21F are sectional views sequentially showing process steps of a method of fabricating a PMOS transistor according to the second embodiment of the present invention;

Figs. 22A to 22C are sectional views sequentially showing process steps of a conventional method of fabricating an NMOS transistor; and

Figs. 23A to 23C are sectional views sequentially showing process steps of a conventional method of fabricating a PMOS transistor.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The next paragraphs will specifically describe preferred embodiments of the present invention referring to the attached drawings.

(Basic Principle of the Invention)

First the basic principle of the present invention will be explained.

Off-leakage current of MOS transistor varies with impurity concentration in its channel (channel dose or pocket dose). In the conventional MOS transistors, a larger channel impurity concentration resulted in a smaller off-leakage current, so that a method of raising the channel impurity concentration has conventionally been adopted in order to suppress the short-channel effect. It has, however, been known as described in the above that the off-leakage current could not be reduced beyond a specific value even if the channel impurity concentration was increased when the gate length was extremely shortened, particularly to as short as 100 nm or below.

Our extensive researches aimed at finding out causes for this problem revealed the following facts. Fig. 1 is a sectional view for explaining types of off-leakage current in an NMOS transistor.

In an exemplary case of OFF status of the NMOS transistor, gate electrode 5 formed on a semiconductor substrate 1 while placing a gate insulating film 4 in between is applied with 0 V, a source region 2 formed in the surficial portion of the semiconductor substrate 1 again with 0 V, the semiconductor substrate 1 again with 0 V, and a drain region 3 formed in the surficial portion of the semiconductor substrate 1 with 1.2 V.

In this status, a source-drain (SD) leakage current flows between the source region 2 and the drain region 3, a gate-drain (GD) tunnel leakage current flows between the gate electrode 5 and the drain region 3, and a body-drain (BD) leakage current flows between the semiconductor substrate 1 and the drain region 3. The off-leakage current is a total of these leakage components.

A relation between the channel impurity concentration and off-leakage current in a PMOS transistor is shown in Fig. 2. Under a gate length such as being owned by the conventional MOS transistors, a certain level of channel impurity concentration was enough to suppress the off-leakage current to a permissible level. In this range, as shown in Fig. 2, the SD leakage current has an extremely large contribution whereas the BD leakage current has only an extremely small contribution, so that raising of the channel impurity concentration readily resulted in a lowered SD leakage current, and consequently in a suppressed off-leakage current.

Although it has been considered that a larger channel impurity concentration is necessary for shortening the gate length, a larger channel impurity concentration undesirably increases contribution of the BD leakage current, and raises the off-leakage current against expectation. That is, as indicated by a solid line in Fig. 2, the off-leakage current has a minimum value.

This indicates that it is no more possible to reduce the off-leakage current only simply by raising the channel impurity concentration, which has been a conventional practice, for MOS transistors having a gate length of as short as 100 nm or less.

The present inventor carried out extensive investigations into reduction in the electric field in the vicinity of the channel, and conceived that the BD leakage current in the PMOS transistor can be suppressed by intentionally using P, which has a large coefficient of diffusion, for formation of the pocket layer, and that in the NMOS transistor can be suppressed by using P for formation of the extension layer.

Fig. 3 is a graph showing relations between channel impurity concentration and off-leakage current, as compared between an As pocket and a P pocket. As shown in Fig. 3, in the PMOS transistor, the BD leakage current becomes lower for the case where the P pocket is used (two-dot chain line), rather than for the case where the As pocket is used (solid line), and consequently the minimum value of the off-leakage current decreases to a corresponding degree. This means that the off-leakage current can be reduced by raising the channel impurity concentration. Also for the NMOS transistor, similar

effect can be expected by using P extension layer in place of the conventional As extension layer.

(Effects in N-Channel MOS Transistor)

Next, effects in the P extension layer in the NMOS transistor will be explained. Fig. 4 is a graph showing relations of gate length and threshold voltage V_{th} of the NMOS transistor having the As extension layer. Fig. 4 shows results of the measurement of the NMOS transistor fabricated by using B for forming the pocket layer, As for forming the extension layer, and P for forming the source and the drain. In Fig. 4, plots ▲, ● and ◆ differ from one another in dose for the pocket layer, where doses represented by plots ● and ◆ are 1.5 times and 2 times as large as dose represented by plot ▲, respectively.

As shown in Fig. 4, the gate length longer than 115 nm (0.115 μm) or around resulted in a relatively small variation in the threshold voltage V_{th} with changes in the gate length, irrespective of the dose. The gate length shorter than 100 nm (0.1 μm), however, resulted in a larger variation (roll-off) in the threshold voltage with changes in the gate length, and in a more distinct short-channel effect.

For the case where the As extension layer was used, it was also found that a gate length of 115 nm resulted in a drain current I_d (off-leakage current) of 10^{-11}(A/μm) or around at a gate voltage V_g of 0 V, even under a low dose of the pocket layer as shown in Fig. 5, whereas a gate length of 80 nm resulted in a large variation in the off-leakage current with dose of the pocket layer which was increased to raise the threshold voltage as shown in Fig. 6. In Figs. 5 and 6, the solid line, broken line and two-

dot chain line indicate results obtained under the same doses as expressed by plots ▲, and ◆ in Fig. 4, respectively. The same will apply also to Figs. 7 and 8.

In short, for the case where the As extension layer was used, as shown in Figs. 5 and 6, even a dose capable of fully suppressing the off-leakage current under a gate length of 115 nm (solid line) was found to result in increase in the off-leakage current by a single or more orders of magnitude under a gate length of 80 nm, where even 1.5 times as much as the dose (broken line) and twice as much as the dose (two-dot chain line) were unsuccessful in fully suppressing the off-leakage current, showing a technical limit for the reduction in the off-leakage current.

Fig. 7 is a graph showing BD leakage component in the drain current I_d shown in Fig. 6. In Fig. 7, the thick lines indicate the BD leakage current, and in more detail, the thick solid line, thick broken line and thick two-dot chain line indicate BD leakage currents expressed by the solid line, broken line and two-dot chain line in Fig. 6, respectively. It was found that the BD leakage current for the case where the As extension layer was used increased as the dose of the pocket layer increased.

In contrast to this, use of the P extension layer in place of the As extension layer for the NMOS transistor is successful in suppressing increase in the BD leakage current with increase in the dose of the pocket layer. Fig. 8 is a graph showing relations between gate voltage V_g and drain current I_d in the NMOS transistor having the P extension layer. Results shown in Fig. 8 are obtained

under a gate length of 80 nm, similarly to those shown in Figs. 6 and 7.

As shown in Fig. 8, when the P extension layer was used, the BD leakage current was found to be stabilized at a low value without showing increase. It was concluded that raising of the dose of the pocket layer was successful in suppressing the SD leakage current, and thereby in suppressing the off-leakage current.

For reference, Fig. 9 is a graph showing relations between gate length and threshold voltage V_{th} of the NMOS transistor having the P extension layer. Plots ▲, ● and ◆ in Fig. 9 respectively indicate results obtained under the same conditions used under the same symbols in Fig. 4. As is clear from Fig. 9, the roll-off was observed even when the P extension layer was used if the gate length was as short as 80 nm or around. However, even in this range of the gate length, the use of the P extension layer made it possible to reduce the off-leakage current by raising the dose of the pocket layer, that is, channel impurity concentration as shown in Fig. 8.

When the P extension layer is formed, it is necessary to carry out the ion implantation after forming a thin sidewall insulating film on the lateral portions of the gate electrode, rather than forming the P extension layer on both sides of the gate electrode in a self-aligned manner under masking only by such gate electrode. This is because P has a larger coefficient of diffusion than As has. Fig. 10 is a graph showing relations between gate length and threshold voltage V_{th} of the NMOS transistor having the P extension layer, as compared between presence and absence of the thin sidewall, and Fig.

11 is a graph showing relations between gate length and off-leakage current I_{off}, as compared between presence and absence of the thin sidewall. Plots ▲ and ◆ in Figs. 10 and 11 indicate results obtained in the absence and presence of the thin sidewall insulating film, respectively. As is clear from Figs. 10 and 11, in the absence of the thin side wall insulating film (▲), the NMOS transistor showed a more distinct roll-off and a large off-leakage current if the gate length is 100 nm or shorter. In an exemplary case with a gate length of 80 nm or around, the presence of the thin sidewall insulating film (◆) resulted in the off-leakage current smaller by a single or more orders of magnitude as compared with the case in the absence of the thin sidewall insulating film (▲).

(Effects in P-Channel MOS Transistor)

Next, effects in the P pocket layer in the PMOS transistor will be explained. Fig. 12 is a graph showing relations of gate length and threshold voltage V_{th} of the PMOS transistor having the As pocket layer. The figure shows results of the measurement of the PMOS transistor fabricated by using As for forming the pocket layer, B for forming the extension layer, and B for forming the source and the drain. In Fig. 12, plots ▲, ● and ◆ differ from each other in dose for the pocket layer, where doses represented by plots ● and ◆ are 2 times and 3 times as large as dose represented by plot ▲, respectively.

As shown in Fig. 12, the gate length longer than 115 nm (0.115 μm) or around resulted in a relatively small variation in the threshold voltage V_{th} with changes in the gate length, irrespective of the dose. The gate length

shorter than 100 nm (0.1 μm), however, resulted in a larger variation (roll-off) in the threshold voltage with changes in the gate length, and in a more distinct short-channel effect. These trends are similar to those for the aforementioned NMOS transistor.

For the case where the As pocket layer was used, it was also found that a gate length of 115 nm resulted in a drain current I_d (off-leakage current) of 10^{-11}(A/μm) or around even under a low dose of the pocket layer as shown in Fig. 13, whereas a gate length of 80 nm resulted in a large variation in the off-leakage current with dose of the pocket layer as shown in Fig. 14. In Figs. 13 and 14, the solid line, broken line and two-dot chain line indicate results obtained under the same doses as expressed by plots ▲, ● and ◆ in Fig. 12, respectively. The same will apply also to Figs. 15, 16 and 17 below.

For the case where the As pocket layer was used, as shown in Fig. 14, a gate length of 80 nm successfully resulted in an off-leakage current reduced to a certain extent by raising the dose of the pocket layer, but the off-leakage current could not be reduced even if the dose was further raised, showing a technical limit for the reduction in the off-leakage current.

Fig. 15 is a graph showing BD leakage component in the drain current I_d shown in Fig. 14. In Fig. 15, the thick lines indicate the BD leakage current, and in more detail, the thick solid line, thick broken line and thick two-dot chain line indicate BD leakage currents expressed by the solid line, broken line and two-dot chain line in Fig. 14, respectively. It was found that the BD leakage

current for the case where the As pocket layer was used increased as the dose of the pocket layer increased.

In contrast to this, use of the P pocket layer in place of the As pocket layer for the PMOS transistor is successful in suppressing increase in the BD leakage current with increase in the dose of the pocket layer. Fig. 16 is a graph showing relations between gate voltage V_g and drain current I_d in the PMOS transistor having the P pocket layer. Results shown in Fig. 16 are obtained under a gate length of 80 nm, similarly to those shown in Figs. 14 and 15.

As shown in Fig. 16, when the P pocket layer was used, the BD leakage current was found to be stabilized at a low value without showing increase. It was concluded that raising of the dose of the pocket layer was successful in suppressing the SD leakage current, and thereby in suppressing the off-leakage current.

For reference, Fig. 17 is a graph showing relations of gate voltage V_g and drain current I_d of the PMOS transistor having a P pocket layer and a gate length of 115 nm. As is known from comparison between Figs. 13 and 17, the effect of reducing the BD leakage current as a consequence of reduction in the off-leakage current was obtained also when the gate length was 115 nm.

Again for reference, Fig. 18 is a graph showing relations between gate length and threshold voltage V_{th} of the PMOS transistor having the P pocket layer. Plots ▲, ● and ◆ in Fig. 18 respectively indicate results obtained under the same conditions used under the same symbols in Fig. 12. As is clear from Fig. 18, the roll-off was observed even when the P pocket layer was used if the gate

length was as short as 80 nm or around. However even in this range of the gate length, the use of the P pocket layer made it possible to reduce the off-leakage current by raising the dose of the pocket layer, that is, channel impurity concentration as shown in Fig. 16.

It is to be noted that the N-type impurity in the pocket layer of the PMOS transistor is not always necessarily composed of P only, but may contain As together therewith. Studies by the present inventor on relations between As ratio and off-leakage current gave results shown in Fig. 19. The pocket was successful in showing a fully reduced off-leakage current similarly to as achieved by the P pocket, when the As ratio is less than 0.7 (70%) to the total N-type impurity in the pocket layer, or in other words, when the P ratio is 0.3 (30%) or more. Similar results were obtained also for the NMOS transistor, where the extension layer of the NMOS transistor is not always necessarily composed of P only, but may contain As together therewith. In this case, the P ratio of 0.5 (50%) or more was successful in fully reducing the off-leakage current similarly to as achieved by the P extension layer.

(First Embodiment)

Next paragraphs will describe a first embodiment of the present invention. It is to be noted that the configuration of the semiconductor device will be explained in combination with a method of fabrication therefor. The first embodiment relates to fabrication of a semiconductor device having an NMOS transistor. Figs. 20A to 20G are sectional views sequentially showing process steps of a method of fabricating the semiconductor

device according to the first embodiment of the present invention.

In the first embodiment, first as shown in Fig. 20A, a gate insulating film 12 and a gate electrode 13 are formed on a semiconductor substrate 11 such as silicon substrate having a P-type well preliminarily formed in the surficial portion thereof. The length of the gate electrode 13 (gate length) is adjusted to 100 nm or shorter, for example.

Next, as shown in Fig. 20B, a P-type impurity such as boron (B) is implanted to thereby form a pair of P-type pocket layers (P-type impurity-diffused layers) 14 in the surficial portion of the semiconductor substrate 11. The ions herein are implanted by oblique ion implantation which is effected from four directions normal to one another in a plan view, for example, at an implantation energy of 5 to 10 keV, and a dose per direction of 3×10^{12} to 1.8×10^{13} cm^{-2}.

Next, as shown in Fig. 20C, a pair of thin sidewall insulating films (a first sidewall insulating films) 15 are formed on the lateral portions of the gate insulating film 12 and the gate electrode 13. The thickness of the thin sidewall insulating film 15 is, for example, adjusted to 10 nm or around. The thickness of the thin sidewall insulating film 15 less than 5 nm may undesirably lower the threshold voltage because the roll-off becomes actualized. On the other hand, the thickness of the thin sidewall insulating film 15 exceeding 15 nm may results in an elevation of the on-resistance due to an increased parasitic resistance. Therefore the thickness of the thin sidewall insulating film 15 preferably falls within a

range from 5 to 15 nm or around. It should be noted that the pair of thin sidewall insulating films 15 may be formed before the P-type impurity is implanted to thereby form the pair of P-type pocket layers 14.

Thereafter as shown in Fig. 20D, phosphorus (P) ion is implanted to thereby form a pair of N-type extension layers (first N-type impurity-diffused layers) 16 in the surficial portion of the pocket layers 14. The ions herein are implanted by ion implantation which is effected from the direction normal to the surface of the semiconductor substrate 11. The implantation energy is set to 1 to 2.5 keV, and the dose to 5×10^{14} to 2×10^{15} cm^{-2}, for example.

Next, an insulating film, a silicon oxide film, for example, is formed on the entire surface, and is then anisotropically etched so as to leave it only on the lateral portion of the thin sidewall insulating film 15, to thereby form a pair of sidewall insulating films (second sidewall insulating films) 17 as shown in Fig. 20E. The thickness of the sidewall insulating film 17 is, for example, adjusted to 75 nm or around. The thickness of the sidewall insulating film 17 is therefore wider than that of the sidewall insulating film 15.

Thereafter, as shown in Fig. 20F, an N-type impurity ion, phosphorus ion, for example, is implanted at a high concentration to thereby form a pair of deep N-type source-and-drain diffusion layers (second N-type impurity-diffused layers) 18 in the surficial portion of the semiconductor substrate 11. The ion implantation herein is effected, for example, from the direction normal to the surface of the semiconductor substrate 11. The

implantation energy is set to 4 to 10 keV, and the dose to 6×10^{15} to 1.2×10^{16} cm^{-2}, for example. The depth of the N-type source-and-drain diffused layer 18 is larger than that of the N-type extension layer 16. After the ion implantation, annealing is carried out so as to activate the implanted impurity.

Thereafter, the semiconductor device is completed as shown in Fig. 20G by forming an interlayer insulating film 19, forming contact holes 20 so as to penetrate the interlayer insulating film 19 to reach the N-type source-and-drain diffusion layers 18, filling the contact holes 20 with a conductive material 21, forming wirings (not shown), and so on.

The thus-fabricated semiconductor device has a configuration shown in Fig. 20G.

According to the above-described first embodiment of the present invention, the N-type extension layer 16 is formed by ion implantation of phosphorus, which has a larger coefficient of diffusion than As has, while using the thin sidewall insulating film 15 as an off-set film, so that a strong electric field is prevented from generating in the vicinity of the channel even if the gate length is as short as 100 nm or less. This is successful in suppressing the BD leakage current, and consequently in suppressing the off-leakage current.

(Second Embodiment)

Next paragraphs will describe a second embodiment of the present invention. It is to be noted again that the configuration of the semiconductor device will be explained in combination with a method of fabrication therefor. The second embodiment relates to fabrication of

a semiconductor device having a PMOS transistor. Figs. 21A to 21F are sectional views sequentially showing process steps of a method of fabricating the semiconductor device according to the second embodiment of the present invention.

In the second embodiment, first as shown in Fig. 21A, a gate insulating film 32 and a gate electrode 33 are formed on a semiconductor substrate 31 such as silicon substrate having an N-type well preliminarily formed in the surficial portion thereof. The length of the gate electrode 33 (gate length) is adjusted to 100 nm or shorter, for example.

Next, as shown in Fig. 21B, phosphorus is implanted to thereby form a pair of N-type pocket layers (N-type impurity-diffused layers) 34 in the surficial portion of the semiconductor substrate 31. The ions herein are implanted by oblique ion implantation which is effected from four directions normal to one another in a plan view, at an implantation energy of 15 to 30 keV, and a dose per direction of 3×10^{12} to 1.5×10^{13} cm^{-2}, for example.

Next as shown in Fig. 21C, a P-type impurity ion, boron (B) ion, for example, is implanted to thereby form a pair of P-type extension layers (first P-type impurity-diffused layers) 36 in the surficial portion of the pocket layers 34. The ion implantation herein is effected, for example, from the direction normal to the surface of the semiconductor substrate 31. The implantation energy is set to 0.2 to 0.5 keV, and the dose to 5×10^{14} to 2×10^{15} cm^{-2}.

Next, an insulating film, a silicon oxide film, for example, is formed on the entire surface, and is then anisotropically etched so as to leave it only on the

lateral portions of the gate insulating film 32 and the gate electrode 33, to thereby form a pair of sidewall insulating films 37 as shown in Fig. 21D. The thickness of the sidewall insulating film 37 is adjusted to 75 nm or around, for example.

Thereafter, as shown in Fig. 21E, a P-type impurity ion, boron ion, for example, is implanted at a high concentration to thereby form a pair of deep P-type source-and-drain diffusion layers (second P-type impurity-diffused layers) 38 in the surficial portion of the semiconductor substrate 31. The ion implantation herein is effected, for example, from the direction normal to the surface of the semiconductor substrate 31. The implantation energy is set to 3 to 6 keV, and the dose to 4×10^{15} to 6×10^{15} cm^{-2}, for example. The depth of the P-type source-and-drain diffused layer 38 is larger than that of the P-type extension layer 36. After the ion implantation, annealing is carried out so as to activate the implanted impurity.

Thereafter, the semiconductor device is completed as shown in Fig. 21F by forming an interlayer insulating film 39, forming contact holes 40 so as to penetrate the interlayer insulating film 39 to reach the P-type source-and-drain diffusion layers 38, filling the contact holes 40 with a conductive material 41, forming wirings (not shown), and so on.

The thus-fabricated semiconductor device has a configuration shown in Fig. 21F.

According to the second embodiment of the present invention, the P-type pocket layer 34 is formed by ion implantation of phosphorus, so that a strong electric

field is prevented from generating in the vicinity of the channel even if the gate length is as short as 100 nm or less. This is successful in suppressing the BD leakage current, and consequently in suppressing the off-leakage current, similarly to as in the first embodiment.